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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,093	07/28/2003	Robert J. Royer	P16418	6380

45209 7590 03/03/2009

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EXAMINER	
CHOE, YONG J	
ART UNIT	**PAPER NUMBER**
2185	

MAIL DATE	DELIVERY MODE
03/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,093	ROYER, ROBERT J.	
	Examiner	Art Unit	
	YONG CHOE	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/07/2008, 04/23/2008 & 01/22/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/629,093 has a total of 21 claims pending in the application. There are 6 independent claims (e.g., claim 1,8,10,12,13 and 20) and 15 dependent claims, all of which are ready for examination by the examiner.

Response to Arguments

2. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/23/2008 has been entered.

Information Disclosure Statement

4. As required by M.P.E.P. 609 (C), the applicant's submission of the information Disclosure Statement dated 02/07/2008, 04/23/2008 & 01/22/2009 are acknowledged by the examiner and the cited references have been

considered in the examination of the claims now pending. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 5, 8, 10, 12, 13, 17 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Syed et al. (US Publication No.: US 2002/0108021)** in view of **Rixner et al. (US Patent No.: US 6,016,531)**.

Regarding independent claims 1,8,10,12 and 20, Syed discloses a method in a Constant Access Time Bounded (CATB) cache (i.e., the applicant did not differentiate the claimed CATB cache from any regular cache. Any well-known cache memory reads on the CATB cache), comprising:

reserving a first number (i.e., one of the "M" ways of the cache) of unallocated lines (i.e., disabled) in the cache ([0083]: a section of the cache is temporarily disabled), the first number ([0083]: one of the "M" ways of the cache) being less than the number of lines in the cache ([0083]: the other “M-1”

ways of the cache) ([0083]: e.g., if there are 4 ways cache, one way is disabled and the other three ways are enabled); and

if data needs to be inserted into the cache, selecting a line from the lines reserved; storing the data in the line; and inserting the line into a search group of the CATB cache ([0083]: After the disabled section of the cache has been unloaded and/or pre-loaded it may then be re-enabled for normal operation. One section is TEMPORARILY disabled and it becomes the enabled cache area so that the area is searchable by CPU. Thus the enabled area is analogous to search group of the CATB cache.), wherein a constant number of non-pinned lines are maintained within the search group ([0083]: e.g., if there are 4 ways cache, one way is disabled and the other three ways are enabled. Thus, a constant number (i.e., three ways) of enabled cache area are maintained).

Syed further teaches a system comprising: a processor (Fig.1: core processor 102); a disk (Fig.1: memory 108) communicatively coupled to the processor (Fig.1: core processor 102); a); and an N-way set associative cache implemented in non-volatile memory ([0083]: “M” ways of cache).

However, Syed do not specifically teach reserving cache lines for pinned data.

Rixner teaches reserving cache lines for pinned data (col.8, lines 56-59: A separate region within cache memory 14 is reserved for the operating system (OS) and is held or pinned such that the OS is available for media use at any time).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate reserving separate cache region for pinned data as taught by Rixner into the high performance cache of Syed in order to reserve private access data (i.e., pinned data) so that the data is available at any time.

Regarding claims 5 and 17, Syed teaches wherein inserting the line into a search group of the cache further comprises: indicating that the line is allocated and using a tag of the line to map the line to a search group of the cache ([0083]: enabled cache line is always allocated and searchable); Rixner teaches indicating that the line is pinned (col.8, lines 56-59: A separate region within cache memory 14 is reserved for the operating system (OS) and is held or pinned);

7. **Claims 6 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Syed et al. (US Publication No.: US 2002/0108021)** in view of **Rixner et al. (US Patent No.: US 6,016,531)** and further in view of **AAPA (Applicant Admitted Prior Art)**.

Regarding claims 6 and 18, Syed and Rixner do not specifically teach the CATB cache is implemented as a set-associative cache; each search group of the cache is a set of the cache; and inserting the line into a search group of the cache further comprises: using the address of the data as the tag of the line;

performing a modulus operation between the tag and the number of sets (N) in the cache (the tag MOD N) to map the tag to a set of the cache; performing a search based on the tag of the line; and inserting the line into a dynamic data structure that represents the set.

However, AAPA teaches the CATB cache is implemented as a set-associative cache; each search group of the cache is a set of the cache; and inserting the line into a search group of the cache further comprises: using the address of the data as the tag of the line; performing a modulus operation between the tag and the number of sets (N) in the cache (the tag MOD N) to map the tag to a set of the cache; performing a search based on the tag of the line; and inserting the line into a dynamic data structure that represents the set (Page 2-3: [02]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the CATB cache as taught by AAPA into the high performance cache of Syed as modified by Rixner because any element on a disk can be quickly mapped to a set in the cache.

8. **Claims 2 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Syed et al. (US Publication No.: US 2002/0108021)** in view of **Rixner et al. (US Patent No.: US 6,016,531)** and in further view of **Norman (US Patent No.: US 6,292,868)**.

Regarding claims 2 and 14, Syed and Rixner do not specifically teach wherein each line of the cache is stored in non-volatile memory.

However, Norman teaches wherein each line of the cache is stored in non-volatile memory (col.6, lines 15-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate each line of the cache is stored in non-volatile memory as taught by Norman into the high performance cache of Syed as modified by Rixner in order to increase speed and reliability (col.6, lines 14-16).

9. **Claims 3, 4, 15 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Syed et al. (US Publication No.: US 2002/0108021)** in view of **Rixner et al. (US Patent No.: US 6,016,531)** and in further view of **Norman (US Patent No.: US 6,292,868)** and **Wong (US Patent No.: US 7,130,979)**.

Regarding claims 3 and 15, Syed, Rixner and Norman do not specifically teach recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a search group of the cache; and if the line is not allocated, inserting the line into a pool of free lines; and in a second phase of recovery, for each search group determining the number of pinned lines in the search group; and adding at least one line from the pool of free lines to each search group that has at least one pinned line.

However, Wong teaches recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a search group of the cache; and if the line is not allocated, inserting the line into a pool of free lines; and in a second phase of recovery, for each search group determining the number of pinned lines in the search group; and adding at least one line from the pool of free lines to each search group that has at least one pinned line (Fig.9, col.9, lines 50-67 and col.10, lines 1-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate recovering system as taught by Wong into the high performance cache of Syed as modified by Rixner and Norman in order to ensure that valid volume definition is available even in the event of a power loss (col.4, lines 47-48).

Regarding claims 4 and 16, Wong teaches wherein the cache is a disk cache in a processor based system (col.1, lines 55-58).

10. **Claims 7 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Syed et al. (US Publication No.: US 2002/0108021)** in view of **Rixner et al. (US Patent No.: US 6,016,531)** and in further view of **AAPA (Applicant Admitted Prior Art)** and **Mandal et al. (US Patent No.: US 6,983,465).**

Regarding claims 7 and 19, Syed, Rixner and AAPA do not specifically teach wherein indicating that the line is pinned further comprises modifying metadata associated with the line to indicate that the line is pinned.

However, Mandal teaches wherein indicating that the line is pinned further comprises modifying metadata associated with the line to indicate that the line is pinned (Fig.8 and col.13, lines 36-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate managing data caching of Mandal into the high performance cache of Syed as modified by Rixner and AAPA in order to view and control the system (col.2, line 29).

11. **Claims 9, 11 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Syed et al. (US Publication No.: US 2002/0108021)** in view of **Rixner et al. (US Patent No.: US 6,016,531)** and in further view of **Wong (US Patent No.: US 7,130,979)**.

Regarding claims 9, 11 and 21, Syed and Rixner do not specifically teach recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a set of the cache using a mapping based on the tag associated with the line; and if the line is not allocated, inserting the line into a pool of unallocated lines; and

in a second phase of recovery, for each set in the cache determining the number of pinned lines in the set using the metadata associated with each line in the set; and moving one or more lines from the pool of unallocated lines to each set that has at least one pinned line so that the number of non-pinned lines in each set is approximately the same.

However, Wong teaches recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a set of the cache using a mapping based on the tag associated with the line; and if the line is not allocated, inserting the line into a pool of unallocated lines; and in a second phase of recovery, for each set in the cache determining the number of pinned lines in the set using the metadata associated with each line in the set; and moving one or more lines from the pool of unallocated lines to each set that has at least one pinned line so that the number of non-pinned lines in each set is approximately the same (Fig.9, col.9, lines 50-67 and col.10, lines 1-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate recovering system as taught by Wong into the high performance cache of Syed as modified by Rixner in order to ensure that valid volume definition is available even in the event of a power loss (col.4, lines 47-48).

Citations of Relevant Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takahashi et al. (US Patent No.: US 6,434,666) discloses memory control apparatus and method for storing data in a selected cache memory based on whether a group or slot number is odd or even.

Conclusion

13. Any inquiry concerning this comm1unication should be directed to **Yong Choe** at telephone number **571-270-1053** or email to **yong.choe@uspto.gov**. The examiner can normally be reached on M-F 9:30am to 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Sanjiv Shah** can be reached on **571-272-4098**. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-irect.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Yong Choe/
Examiner, Art Unit 2185

/Tuan V. Thai/
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